## REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-5, 9-10, 15 and 79-93 are presently active, Claims 6-8, 11-14, 16-78 have been previously canceled without prejudice, Claims 1, 4, 9-10, 15, 79-80 and 86-87 are amended, and Claims 91-93 are added by the present amendment. No new matter is added.

In the outstanding Office Action, Claims 15, 79 and 83-85 were rejected under 35 U.S.C. § 102(e) as anticipated by Yamashita (USP 5,875,100). Claims 1, 4-5 and 9 were rejected under 35 U.S.C. § 103(a) as unpatentable over Mowatt et al. (USP 6,306,670) in view of Yamashita. Claims 2-3 were rejected under 35 U.S.C. § 103(a) as unpatentable over Mowatt et al. in view of Yamashita, and further in view of Sakaguchi et al. (USP 5,837,624). Claims 2-4 and 10 were rejected under 35 U.S.C. § 103(a) as unpatentable over Mowatt et al. in view of Yamashita, and further in view of Ehman et al. (USP 6,021,050). Claims 81-82 were rejected under 35 U.S.C. § 103(a) as unpatentable over Yamashita in view of Sakaguchi et al. Claims 80-82 and 86-90 were rejected under 35 U.S.C. § 103(a) as unpatentable over Yamashita in view of Ehman et al.

Regarding the rejection of the pending claims under, Applicants respectfully submit that the outstanding grounds for rejection is overcome, because in Applicants' view, independent Claims 1, 15 and 86 patentably distinguishes over the applied references as discussed below.

Claim 1 is amended to recite, *inter alia*, "a chip capacitor having external capacitor electrodes, the chip capacitor formed in the opening of the second resin substrate," "the opening covered with the second surface of the first resin substrate," "a first conductive pad formed on the second surface of the first resin substrate and connected to one of the external capacitor electrodes of the chip capacitor" and "a second conductive pad formed on the

second surface of the first resin substrate and connected to the other of the external capacitor electrodes of the chip capacitor."

The outstanding Office Action states that Mowatt et al. discloses a semiconductor die (56) formed in the opening (14) of the second resin substrate (10) and first and second conductive pads (130, 132) formed on (and in) a surface of the first resin substrate and connected to electrodes (60, 62) of the die (Office Action at page 4, 8-11).

However, Claim 1 is amended to recite that the first and second conductive pads are formed on the second surface of the first resin substrate, the opening covered with the second surface of the first resin substrate. Instead, in Mowatt et al., the interconnect structures (130, 132), which the outstanding Office Action states corresponds to the "conductive pads" in Claim 1, are not formed on the surface the laminate layer (126), the surface covering the opening in which the semiconductor die (56) is formed.

Further, the outstanding Office Action acknowledges that Mowatt et al. does not disclose that the semiconductor die (56) is a capacitor (Office Action at page 4, lines 15-16). Instead, the outstanding Office Action relies on Yamashita to remedy the deficiencies, stating that Yamashita shows a PCM comprising a semiconductor chip, which is a capacitor formed in the opening (21) (Office Action at page 4, lines 17-19). Applicants respectfully disagree.

Yamashita describes "[i]n place of the semiconductor chip 10, a rectangular module obtained by sealing a resistor and a capacitor in a ceramic member ... can be used." However, Yamashita merely teaches that the semiconductor chip 10 can be a rectangular module including a resistor and a capacitor, and Yamashita does not suggest that the semiconductor chip 10 is ***a chip capacitor having external capacitor electrodes***.

In addition, Mowatt et al. does not disclose a chip capacitor having external capacitor electrodes.

Thus, even the combination of Yamashita and Mowatt et al. fails to teach or suggest "a chip capacitor having external capacitor electrodes, the chip capacitor formed in the opening of the second resin substrate," "the opening covered with the second surface of the first resin substrate," "a first conductive pad formed on the second surface of the first resin substrate and connected to one of the external capacitor electrodes of the chip capacitor" and "a second conductive pad formed on the second surface of the first resin substrate and connected to the other of the external capacitor electrodes of the chip capacitor," as recited in Claim 1.

Accordingly, independent Claim 1 patentably distinguishes over the applied references. Therefore, Claim 1 and the pending Claims 2-5, 9-10, 84-85 and 91 directly or indirectly dependent from Claim 1 are believed to be allowable.

Next, Claim 15 recites, *inter alia*, "said first resin substrate and said ship capacitor are coupled to each other by an insulating bonding agent and a coefficient of thermal expansion of the insulating bonding agent is lower than a coefficient of thermal expansion of said first resin substrate."

The outstanding Office Action states that Yamashita discloses first resin substrate and the ceramic capacitor (10) are coupled to each other by an insulating bonding agent (sealing layer 30) and having a coefficient of thermal expansion (CTE) lower than a CTE of the first substrate (on top of the sealing layer 30) (Office Action at paragraph 2). Applicants respectfully disagree.

Yamashita describes that in order to add the build-up layers 30 and the wiring patterns 51 on the outer layers, it suffices to repeat the steps shown in Figs. 1C to 1F, enabling formation of a multiplayer structure easily (Yamashita at col. 4, lines 45-48). That is, Yamashita suggests that the build-up layers 30 are composed of a same material and formed by a same process. Therefore, the sealing layer 30, which the outstanding Office Action

assumes corresponds to "an insulating bonding agent" in Claim 15, has the same CTE as the layer on top of the sealing layer 30.

Thus, Yamashita fails to teach or suggest "said first resin substrate and said chip capacitor are coupled to each other by an insulating bonding agent and a coefficient of thermal expansion of the insulating bonding agent is lower than a coefficient of thermal expansion of said first resin substrate," as recited in Claim 15.

Accordingly, independent Claim 15 patentably distinguishes over the applied references. Therefore, Claim 15 and the pending Claims 79-83 and 92 directly or indirectly dependent from Claim 15 are believed to be allowable.

Next, Claim 86 recites, *inter alia*, "a core substrate comprising a first resin substrate, ***a second resin substrate having an opening*** and a third resin substrate in a multilayer manner while interposing bonding plates," "a chip capacitor formed in the opening of the second resin substrate, the chip capacitor including a first electrode, a second electrode and a dielectric made of ceramic" and "wherein ***each of said first, second and third resin substrates has a core made of glass cloth and impregnated with a resin***."

That is, ***the second resin substrate having an opening***, in which a chip capacitor including a first electrode, a second electrode and a dielectric made of ceramic is formed, ***has a core made of glass cloth and impregnated with a resin***. By using a substrate made of glass cloth and impregnated with a resin for the second resin substrate, a coefficient of thermal expansion of the second resin substrate is set to close to a coefficient of thermal expansion of the chip capacitor including the dielectric made of ceramic and formed in the second resin substrate. Therefore, even if an internal stress occurs by a difference in the coefficients of thermal expansion of the second resin substrate and the chip capacitor, cracks and separations less occur to the second substrate, making it possible to attain high reliability and prevent the occurrence of migration. Further, the glass cloth in the second resin substrate prevents the

expansion of the cracks. Thus, there can be obtained unexpected advantages to use a glass cloth as a core material of the second resin layer.

The Office Action acknowledges that Yamashita does not disclose the first, second and third resin substrates having a core made of glass cloth and a resin impregnated with a resin (Office Action at page 7, lines 1-5). Instead, the Office Action relies on Ehman et al. to remedy the deficiencies of Yamashita, asserting that Ehman et al. teaches a printed wiring board comprising layers (12, 14 and 16) each made of glass cloth and a resin impregnated with a thermosetting resin (Office Action at page 7, lines 6-8). However, Applicants respectfully traverse the outstanding obviousness rejection, as discussed below.

Initially, Applicants note that to establish a *prima facie* case of obviousness, M.P.E.P. §2143 requires that three criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the references teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references must teach or suggest all the claim elements.

In order to properly combine or modify references for the purpose of the obviousness rejection, *the references must suggest the desirability of a proposed combination or modification beyond the mere fact that references can be combined or modified.*[1] CAFC established that ***substantial evidence*** *of motivation or teaching must be shown for combining or modifying the references,*[2] and also that such modification requires "***clear and particular evidence.***"[3]

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[1] MPEP 2143.01, In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). See also MPEP 2144.08 III stating that "[e]xplicit findings on motivation or suggestion to select the claimed invention should also be articulated in order to support a 35 U.S.C. 103 ground of rejection .... Conclusory statements of similarity or motivation, without any articulated rational or evidentiary support, do not constitute sufficient factual findings."

[2] In re Gartside, 203 F3d 1305, 53 USPQ2d 1769 (Fed. Cir. 2000) (holding that, consistent with the Administrative Procedure Act at 5 USC 706(e), the CAFC reviews the Board's decisions based on factfindings,

Ehman et al. describes that the intermediate layers (18 and 20), in which capacitors (44, 46 and 48) are formed, are made of thermal setting resin (Ehman et al. at column 5, lines 43-46). That is, Ehman et al. does not teach or suggest using a glass cloth as a core material of ***the substrate having an opening, in which a chip capacitor including a dielectric made of ceramic is formed***. Although Ehman et al. describes that a glass cloth is used as a core material of layers (12, 14 and 16), Ehman et al. does not teach or suggest that ***the intermediate layer (18 and 20) accommodating a capacitor (44, 46 and 48)*** comprises a glass cloth as a core material. Since the intermediate layers (18 and 20) do not have a glass cloth as a core material, the structures disclosed in Ehman et al. cannot decrease the generation of cracks and separations in the intermediate layers (18 and 20), in which a capacitor including a dielectric made of ceramic is formed, and cannot attain high reliability and prevent the occurrence of migration.

Further, generally, it is difficult to process a substrate containing a glass cloth as a core material, compared with a substrate having no glass cloth. Therefore, there is no suggestion or motivation in Ehman et al., which merely describes a glass cloth is used as a core material of layers (12, 14 and 16), to modify the printed circuit board (20) of Yamashita, which has an opening to accommodate a semiconductor chip 10, to comprise a glass cloth as a core material.

Thus, even combination of Yamashita and Ehman et al. fails to teach or suggest that the second resin substrate having an opening, in which a chip capacitor including a dielectric

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such as 35 U.S.C. § 103(a) rejections, using the 'substantial evidence' standard because these decisions are confined to the factual record compiled by the Board.).

[3] In re Dembiczak, 175 F3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999) ("We have noted that evidence of a suggestion, teaching, or motivation to combine/modify may flow from the prior art references themselves, the knowledge of one of ordinary skill in the art, or, in some cases, from the nature of the problem to be solved, although 'the suggestion more often comes from the teachings of the pertinent references.' The range of sources available, however, does not diminish the requirement for actual evidence. That is, the showing must be clear and particular.") (emphasis added).

made of ceramic is formed, has a core made of glass cloth and impregnated with a resin. Therefore, Applicants respectfully submit that a *prima facie* case of obviousness is not established.

Accordingly, independent Claim 86 patentably distinguishes over the applied references. Therefore, Claim 86 and the pending Claims 87-90 and 93 directly or indirectly dependent from Claim 86 are believed to be allowable.

Consequently, in view of the present amendment and in light of the above discussions, it is believed that the outstanding rejection has been overcome, and the application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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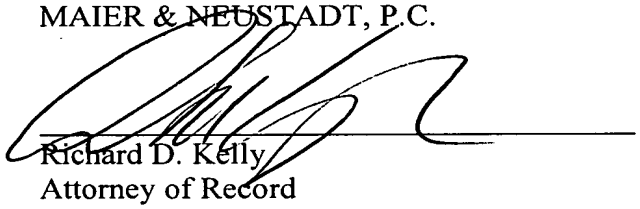

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